G83/2-1 Engineering Recommendation

<table>
<tr><td colspan="5">Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2-1.</td></tr>
<tr><td colspan="2">SSEG Type reference number</td><td colspan="3">DQ170414</td></tr>
<tr><td colspan="2">SSEG Type</td><td colspan="3">Solis-1P3.6K-4G</td></tr>
<tr><td colspan="2">System Supplier name</td><td colspan="3">Ningbo Ginlong Technologies Co., Ltd.</td></tr>
<tr><td colspan="2">Address</td><td colspan="3">No. 57 Jintong Road, Seafront (Binhai) Industrial Park, Xiangshan, Ningbo, Zhejiang, 315712,P.R.China</td></tr>
<tr><td>Tel</td><td colspan="2">(+86) 574 6580 3377</td><td>Fax</td><td>(+86) 574 6578 1606</td></tr>
<tr><td>E:mail</td><td colspan="2">kun.zhang@ginlong.com</td><td>Web site</td><td>www.ginlong.com</td></tr>
<tr><td rowspan="5">Maximum rated capacity</td><td colspan="4">Connection Option</td></tr>
<tr><td>3.6</td><td colspan="3">kW single phase, single, split or three phase system</td></tr>
<tr><td>--</td><td colspan="3">kW three phase</td></tr>
<tr><td>--</td><td colspan="3">kW two phases in three phase system</td></tr>
<tr><td>--</td><td colspan="3">kW two phases split phase system</td></tr>
<tr><td colspan="5">SSEG manufacturer/supplier declaration.
I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2-1.</td></tr>
<tr><td>Signed</td><td></td><td>On behalf of</td><td colspan="2">Ginlong Technologies</td></tr>
</table>

G83/2-1 Appendix 4 Type Verification Test Report

Power Quality. Harmonics. The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1						
SSEG rating per phase (rpp)			3.6	kW	NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.016	0.016	0.045	0.046	1.080	
3	0.076	0.078	0.270	0.276	2.300	
4	0.015	0.016	0.031	0.032	0.430	
5	0.058	0.059	0.131	0.134	1.140	
6	0.014	0.015	0.016	0.016	0.300	
7	0.044	0.045	0.099	0.101	0.770	
8	0.011	0.011	0.021	0.021	0.230	
9	0.035	0.036	0.060	0.062	0.400	
10	0.008	0.008	0.020	0.021	0.184	
11	0.032	0.033	0.062	0.063	0.330	
12	0.011	0.011	0.020	0.020	0.153	
13	0.019	0.020	0.040	0.041	0.210	
14	0.013	0.013	0.018	0.019	0.131	
15	0.030	0.030	0.030	0.030	0.150	
16	0.013	0.013	0.008	0.008	0.115	
17	0.010	0.010	0.021	0.021	0.132	
18	0.008	0.009	0.017	0.017	0.102	
19	0.015	0.015	0.031	0.031	0.118	
20	0.006	0.006	0.023	0.023	0.092	
21	0.018	0.018	0.010	0.011	0.107	0.160
22	0.008	0.008	0.015	0.015	0.084	
23	0.005	0.005	0.017	0.018	0.098	0.147
24	0.008	0.008	0.015	0.016	0.077	
25	0.007	0.008	0.014	0.014	0.090	0.135
26	0.009	0.010	0.029	0.029	0.071	
27	0.015	0.015	0.022	0.022	0.083	0.124
28	0.009	0.009	0.013	0.013	0.066	
29	0.007	0.007	0.010	0.010	0.078	0.117
30	0.005	0.005	0.020	0.020	0.061	
31	0.009	0.010	0.030	0.031	0.073	0.109
32	0.018	0.018	0.037	0.038	0.058	
33	0.012	0.013	0.010	0.010	0.068	0.102
34	0.010	0.010	0.035	0.036	0.054	
35	0.012	0.012	0.017	0.018	0.064	0.096
36	0.007	0.008	0.019	0.019	0.051	
37	0.004	0.004	0.007	0.007	0.061	0.091

38	0.011	0.011	0.027	0.028	0.048	
39	0.019	0.020	0.027	0.028	0.058	0.087
40	0.005	0.005	0.009	0.009	0.046	
Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.						

Power Quality. Voltage fluctuations and Flicker.
The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3

	Starting			Stopping			Running	
	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c	$d_{(t)}$	P_{st}	P_{lt} 2 hours
Measured Values	0.43	0.36	0	0.37	0.24	0	0.056	0.07
Normalised to standard impedance and 3.68kW for multiple units	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65

Test start date	27. June.2018	Test end date	27. June.2018
Test location	Ningbo Ginlong electrical R&D LAB		

Power Quality. DC injection.
The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4

Test power level	10%	55%	100%
Recorded value	15.2mA	13.3mA	16.4mA
as % of rated AC current	0.097%	0.085%	0.104%
Limit	0.25%	0.25%	0.25%

Power Quality. Power factor.
The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2

Test voltage	216.2V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.
Measured value	>0.99	>0.99	>0.99	
Limit	>0.95	>0.95	>0.95	

Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3						
Function	Setting		Trip test		"No trip tests"	
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.55Hz	20s	47.55Hz	20.4s	47.7Hz / 25s	Yes
U/F stage 2	47.05Hz	0.5s	47.05Hz	0.7s	47.2Hz / 19.98s	Yes
					46.8Hz / 0.48s	Yes
O/F stage 1	51.45Hz	90s	51.45Hz	90.5s	51.3Hz / 95s	Yes
O/F stage 2	51.95Hz	0.5s	51.95Hz	0.53s	51.8Hz / 89.98s	Yes
					52.2Hz / 0.48s	Yes

Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						
Function	Setting		Trip test		"No trip tests"	
	Voltage	Time delay	Voltage	Time delay	Voltage /time	Confirm no trip
U/V stage 1	200.1V	2.5s	198	2.8s	204.1V / 3.5s	Yes
U/V stage 2	184V	0.5s	182	0.64s	188V / 2.48s	Yes
					180V / 0.48s	Yes
O/V stage 1	262.2V	1.0s	264	1.3s	258.2V / 2.0s	Yes
O/V stage 2	273.7V	0.5s	275	0.63s	269.7V / 0.98s	Yes
					277.7V / 0.48s	Yes
Note for Voltage tests the Voltage required to trip is the setting ±3.45V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting ±4V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.						

Protection. Loss of Mains test. The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Limit is 0.5 seconds	0.29s	0.38s	0.14s	0.41s	0.28s	0.36s
For Multi phase SSEGs confirm that the device shuts down correctly after the removal of a single fuse as well as operation of all phases.						

Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph1 fuse removed	0.36s	0.32s	0.34s	0.30s	0.32s	0.34s
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph2 fuse removed	0.32s	0.31s	0.42s	0.31s	0.25s	0.32s
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph3 fuse removed	0.32s	0.30s	0.35s	0.33s	0.20s	0.30s
Note for technologies which have a substantial shut down time this can be added to the 0.5 seconds in establishing that the trip occurred in less than 0.5s. Maximum shut down time could therefore be up to 1.0 seconds for these technologies.						
Indicate additional shut down time included in above results.					0.3 ms	
Note as an alternative, inverters can be tested to BS EN 62116. The following sub set of tests should be recorded in the following table.						
Test power and iimbalance	33% -5 Q test 22	66% -5 Q test 12	100% -5 Q test 5	33% +5 Q test 31	66% +5 Q test 21	100% +5 Q test 10
Trip time. Limit is 0.5s	0.34s	0.30s	0.32s	0.35s	0.28s	0.30s

Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+50 degrees		Yes
Negative Vector Shift	50.5Hz	- 50 degrees		Yes

Protection. Frequency change, RoCoF Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6			
Ramp range	Test frequency ramp:	Test Duration	Confirm no trip
Positive Vector Shift	$+0.95Hzs^{-1}$	2.1s	Yes
Negative Vector Shift	$-0.95Hzs^{-1}$	2.1s	Yes

Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5					
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.					
Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
30s	32s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.		Yes	Yes	Yes	Yes

Fault level contribution

Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6					
For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	i_p	--	20ms	5.77V	37.4Apeak
Initial Value of aperiodic current	A	--	100ms	0	0
Initial symmetrical short-circuit current*	I_k	--	250ms	0	0
Decaying (aperiodic) component of short circuit current*	i_{DC}	--	500ms	0	0
Reactance/Resistance Ratio of source*	X/R	--	Time to trip	<20ms	In seconds

Self-Monitoring solid state switching The requirement is specified in section 5.3.1, No specified test requirements.	Yes/or NA
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 seconds.	NA

Additional comments